UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,637	08/28/2003	Shigeki Imai	0756-7192	5558

31780 7590 05/18/2005

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
PARKER, KENNETH	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No. 10/649,637	Applicant(s) IMAI ET AL.	
	Examiner Kenneth A. Parker	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/1/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In each independent claim a first substrate is indicated with elements above it, then further into the claim other substrates are indicated in which it is ambiguous whether those substrates are additional substrates or the first substrate reiterated. Therefore there is no way to determine how many substrates must minimally be present for the claims to be anticipated, and the claims are therefore indefinite.

In claims 8, 16, "deflection plate disposed only nearby said optical shutter" is not understood. First, what is a deflection plate is completely unknown, however by its use it appears to be a polarizer, and second, what is meant by "only nearby" is not understood, and for examining purposes it is assumed to mean that it is located nearby.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 –2, 7-10, 15-18, 23-26, 31-34, 39-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Shannon 5268679.

The reference shows regarding claim 1. An electronic circuit device comprising: a plurality of electronic circuit substrates (each 10 has wires shown) over which either of an optical shutter (each liquid crystal cell) or an optical sensor (each has a sensor) is disposed, or both of them are disposed, wherein said plurality of electronic circuit substrates comprise transparent substrates (the substrates 10 themselves), an optical signal is inputted from an external (light has to get in the device, or the shutters wouldn't do anything and the device wouldn't work, and is therefore inherent), said optical signal which has been inputted is inputted into an optical shutter or an optical sensor over a transparent substrate which is different from said transparent substrates after said optical signal has been transmitted through at least one or more of said transparent substrates, said optical shutter controls transmission and non-transmission of said optical signal (that is what the shutters do), and said optical sensor converts said optical signal into an electric signal by an electronic circuit provided over a same transparent substrate as said optical sensor (the readout matrix creates an electronic signal).

The reference shows regarding claim 2. A device according to claim 1, wherein said electronic circuit comprises a thin film transistor (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 7. A device according to claim 1, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 8. A device according to claim 7, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 9. An electronic circuit device comprising: a plurality of transparent substrates (each 1- has wires shown) over which either of an optical shutter (liquid crystal cell) or an optical sensor (each has a sensor) is disposed, or both of them are disposed, wherein said plurality of transparent substrates have been laminated (they are shown stacked), an optical signal is inputted from an external (it has to come from somewhere or the device wouldn't work), said optical signal which

has been inputted is inputted into an optical shutter or an optical sensor over a transparent substrate which is different from said transparent substrates after said optical signal has been transmitted through at least one or more of said transparent substrates (there are many stacked), said optical shutter controls transmission and non-transmission of light (that is what shutters do), and said optical sensor converts said optical signal into an electric signal by an electronic circuit provided over a same transparent substrate as said optical sensor (that is what sensors to, and the circuit is shown as a readout matrix).

The reference shows regarding claim 10. A device according to claim 9, wherein said electronic circuit comprises a thin film transistor (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 15. A device according to claim 9, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 16. A device according to claim 15, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent

(column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 17. An electronic circuit device comprising a plurality of transparent substrates over which either of an optical shutter or an optical sensor is disposed (each 10 has wire shown and therefore has the LCD and sensor structures), or both of them are disposed, wherein an optical signal is directly inputted into said optical shutter from an external or said optical signal is inputted into said optical shutter after said optical signal has been transmitted through said transparent substrate, in a case where said optical shutter has transmitted said optical signal, the transmitted optical signal is directly inputted into said optical sensor or inputted into said optical sensor after said optical signal has been transmitted through a transparent substrate which is different from said transparent substrates (the signals go through substrates, and strike sensors).

The reference shows regarding claim 18. A device according to claim 17, wherein said electronic circuit comprises a thin film transistor. (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 23. A device according to claim 17, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of

transparent substrates (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 24. A device according to claim 23, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 25. An electronic circuit device comprising: a plurality of transparent substrates over which either of an optical shutter or an optical sensor is disposed (each 10 has wire shown and therefore has the LCD and sensor structures), or both of them are disposed, wherein said optical shutter is controlled by an electronic circuit over a transparent substrate (the driving circuit is shown- see figure 1) , an optical signal inputted from an external is inputted into said optical shutter (it has to come from somewhere, so this limitation is inherent), and whether said optical signal has been transmitted or not is decided, thereby taking out an output signal of said electronic circuit (this is true by definition).

The reference shows regarding claim 26. A device according to claim 25, wherein said electronic circuit comprises a thin film transistor. (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 31. A device according to claim 25, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates. (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 32. A device according to claim 31, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

The reference shows regarding claim 33. An electronic circuit device comprising: a plurality of transparent substrates over which either of an optical shutter or an optical sensor is disposed, or both of them are disposed (each 10 has wires for at least one of sensors and LCD shutters), wherein said transparent substrates have been laminated (they are stacked), said optical shutter is controlled by an electronic circuit provided over said transparent substrate (the driving matrix is shown), an optical signal inputted from an external is inputted into said optical shutter, and whether said optical signal has been transmitted or not is decided, thereby taking out an output signal of said electronic circuit (this is true by definition).

The reference shows regarding claim 34. A device according to claim 33, wherein said electronic circuit comprises a thin film transistor. (column 5-6 and elsewhere list thin film FET, which is a thin film transistor).

The reference shows regarding claim 39. A device according to claim 33, wherein said optical shutter comprises a liquid crystal which is sandwiched between two sheets of transparent substrates. (as shown in figure 2, numerous 10 layers stacked with a liquid crystal layer at its side (column 4, lines 17-34).

The reference shows regarding claim 40. A device according to claim 39, wherein a deflection plate is disposed on said transparent substrate, and said deflection plate is disposed only nearby said optical shutter. The reference shows polarizers adjacent (column 4, lines 1-50), meeting the limitations of this claim as understood in light of the rejection under 112 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-6, 11-14, 19-22, 27-30,35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shannon 5268679 in view of Yamada 5583570, Williams 5491571 Shindo et al 5738731.

Shannon shows the sensor as a photodiode (abstract), but does not indicate what level of crystallinity the circuits and photodiodes are. Note that the term "chip" is taken as met by the reference, as any circuit can be construed as chips. Yamada shows that the range of crystalline from amorphous to single crystal was applicable to

photodoides "a MOSFET photocell and photodiode using a monocrystalline silicon, amorphous silicon, polycrystalline silicon or the like are known." Shindo et al shows that the higher crystallinities had higher cost and manufacturing complexity (cols 7 and 9-10). Williams shows that the higher crystalline had benefits of improved speed (column 2, lines 9-21), and therefore considering the tradeoff cost and manufacturing complexity for the higher levels of crystallinity the level of crystallinity is a result effective for the photdiode and driving circuits. It has been judicially determined that the selection of a result effective variable is at least obvious. Therefore the selection of a particular level of crystallinity, i.e. amorphous (claims 4, 12, 20, 28, 36,) polysilicon (claims 5, 13, 21, 29, 37) or single crystal silicon (claims 3, 6, 11, 14, 19, 22, 27, 30, 35, 38) would have been within the ordinary skill level, and one of ordinary skill would have found motivation, suggestion or reason to select single crystal for the best speed, amorphous for the lowest speed but simplest manufactuing, and polycrystalline for the middle cost and speed tradeoffs for each of the photodiode and driving circuits).

Election/Restrictions

Applicant's election without traverse of group I in the reply filed on 2/22/05 is acknowledged.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mashiko 4988891, Robinson 5383042, and Murphy 5297232 are relevant to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A. Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth A Parker
Primary Examiner
Art Unit 2871